Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application.

1. (Currently Amended) Data transmission system comprising:

a packet switch module comprising a plurality of input ports and a plurality of output ports; and

a memory block (200) located at each crosspoint of said switch module, wherein each couple of one of said input ports and one of said output ports defines a crosspoint, said memory block including

memory control means (210, 212, 234) for determining from the header of a received data packet whether said packet is to be forwarded to the output port associated with said crosspoint; and

a data memory unit (226) for storing at least said data packet into said data memory unit before sending it to said output port, ~~and~~

wherein said memory control means analyzes all the bytes following said header when said header includes a specific configuration indicating that said packet is a multicast address packet preceding a multicast frame, said multicast address packet including information describing a plurality of destination output ports for said multicast frame, wherein said all bytes following the header are analyzed in order to determine, without the use of a routing table, whether the packets of said multicast frame are to be forwarded to said output port associated with said crosspoint.

2. (Original) Data transmission system according to claim 1, further comprising a scheduler (500) associated with each output port for selecting at each clock time a memory block (200) among all memory blocks corresponding to said output port and causing said memory block to forward the data packet stored in the data memory unit (226) of said memory block to said output port when predetermined criteria are met.

3. (Original) Data transmission system according to claim 2, wherein said memory control means includes a header validation control block (216) for determining whether the header of said

packet received from said input port contains said specific configuration indicating that it is a multicast address packet and a memory controller (234) for storing all the packets of said multicast frame which follows said multicast address packet into said data memory unit (226) if said header validation control block has determined that the packets of said multicast frame are to be forwarded to said output port.

4. (Original) Data transmission system according to claim 3, wherein said scheduler (500) sends a validation signal (206) to said header validation control block (216) to authorize said memory controller (234) to store said data packet into said data memory unit (226).

5. (Original) Data transmission system according to claim 4, further comprising an output data block (400) connected to each output port for storing a data packet received from any memory block (200) and transmitting said data packet to said output port under the control of said scheduler (500).

6. (Original) Data transmission system according to claim 5, wherein said output data block (400) includes a data selection block (402) for validating said data packet after receiving a validating signal (206) from said scheduler (500), an output memory unit (406) for storing said data packet and a memory controller (408) for controlling the operation of storing said data packet into said output memory unit and the operation of reading said output memory unit for transmitting said data packet to said output port.

7. (Original) Data transmission system according to claim 6, wherein said packet switch (14) includes a plurality of switch modules, each byte of said multicast address packet following said header being associated with one of said switch modules and defining the addresses of the output ports of said module to which said multicast frame is to be forwarded.

8. (Original) Data transmission system according to claim 7, wherein said packet switch (14) includes a plurality of switch modules and wherein each down switch module includes for each output port an input expansion data block (300) for buffering a data packet received from an expansion bus in (17) connected to an up switch module and corresponding to the same output port as said output port of said down switch module.

9. (Original) Data transmission system according to claim 8, wherein said input expansion data block (300) includes an expansion memory unit (312) for buffering said data packet received from said expansion bus in (17), a header validation block (308) for determining whether the header of said data packet contains the address of the output port associated with said crosspoint and a memory controller (314) for storing said data packet into said expansion memory unit and reading said expansion memory unit to forward it to said output port of said down switch module.

10. (Previously presented) Data transmission system according to claim 9, wherein said scheduler (500) sends a validation signal (206) to said header validation block (308) to authorize said memory controller (314) to store said data packet into said expansion memory unit (312).

11. (Original) Data transmission system according to any one of claims 1 to 10, wherein an overflow signal (236) is sent by said memory block (200) to said scheduler (500) when said memory block overflows.

12. (Original) Data transmission system according to claim 11, further comprising an overflow bus (70) to transport said data packet to said memory block (200) corresponding to said output port after that said scheduler (500) has prevented said data packet from being stored into said memory block which overflows and has selected and validated another memory block which does not overflow.

13. (Previously presented) Data transmission system according to claim 1, further comprising a back-pressure mechanism (900) adapted to send back-pressure signals (922) to input adapters for requesting them to reduce the flow of data packets transmitted to said packet switch (14) when there is too much overflow detected by each scheduler of said packet switch.

14. (Original) Data transmission system according to claim 13, further comprising an overflow mechanism adapted to receive overflow control signals (710) from the schedulers of said packet switch (14) when there is too much overflow and to transmit an overflow signal to said back-pressure mechanism (900).

15. (Previously presented) Data transmission system according to any one of claims 1 to 10, wherein the header of said multicast address packet includes one byte wherein the last significant bits are "100".

16. (Original) Data transmission system according to claim 15, wherein the header of any data packet which is not a multicast address packet includes two bytes in which the first byte contains an identification field and the second byte contains a module address field when said packet switch (14) comprises several packet switch modules.

17. (Currently amended) A data transmission system including:

a switch module having at least two crosspoints;

a memory operatively coupled to each one of the at least two crosspoints; and

a plurality of memory controllers, one of each operatively coupled to each one of the memory, said memory controllers examining a header of a ~~data~~ packet which is forwarded to output ports associated with the coupled crosspoint and ~~examining all bytes said memory control means analyzes~~ analyzing all the bytes following said header when said header includes a specific configuration indicating that said packet is a multicast address packet preceding a multicast frame, said multicast address packet including information describing a plurality of destination output ports

for said multicast frame, wherein said all bytes following the header are analyzed in order to determine, without the use of a routing table, whether the packets of said multicast frame are to be forwarded to said output port associated with the coupled crosspoint.

18. (Previously Presented) The data transmission system of Claim 17 further including at least two adapters operatively coupled to the switch module.

19. (Previously Presented) The data transmission system of Claim 18 further including at least one LAN operatively coupled to each of the adapters.

20. (New) Data transmission system comprising:

a packet switch module;

a memory block (200) located at each crosspoint of said switch module, said memory block including

memory control means (210, 212, 234) for determining from the header of a data packet whether said packet is to be forwarded to the output port associated with said crosspoint;

a data memory unit (226) for storing at least said data packet into said data memory unit before sending it to said output port;

a scheduler (500) associated with each output port for selecting at each clock time a memory block (200) among all memory blocks corresponding to said output port and causing said memory block to forward the data packet stored in the data memory unit (226) of said memory block to said output port when predetermined criteria are met, wherein an overflow signal (236) is sent by said memory block (200) to said scheduler (500) when said memory block overflows; and

an overflow bus (70) to transport said data packet to said memory block (200) corresponding to said output port after said scheduler (500) has prevented said data packet from being stored into said memory block which overflows and has selected and validated another memory block which does not overflow,

wherein said memory control means analyzes all the bytes following said header when said header includes a specific configuration indicating that said packet is a multicast address packet preceding a multicast frame in order to determine whether the packets of said multicast frame are to be forwarded to said output port.